IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended): A non-volatile semiconductor memory device comprising:

a semiconductor body of a first conductivity type;

first and second semiconductor regions of a second conductivity type, formed apart from each other on the semiconductor body;

a gate insulating film formed on the semiconductor body between the first and second semiconductor regions and on the second semiconductor region;

a first stacked gate formed on a gate insulating film on the semiconductor body between the first and second semiconductor regions, ~~with a gate insulating film inserted therebetween,~~ the first stacked gate having a first side surface, a second side surface opposed to the first side surface, and an upper surface;

an interlayer insulating film formed above the semiconductor body;

a contact material buried to be adjacent to the first side surface of the first stacked gate in the interlayer insulating film, the contact material contacting the first semiconductor region;

a first insulating film formed on the second side surface and on the upper surface and on the gate insulating film on the second semiconductor region, but not on the first side surface of the first stacked gate adjacent to the contact material; and

a second insulating film formed on the first side surface adjacent to the contact material and on the first insulating film on the gate insulating film on the second

semiconductor region, the second insulating film having an etch rate slower than that of said first insulating film ~~and covering the entirety of the first insulating film~~.

2. (Currently Amended): The device according to claim 1, wherein the first stacked gate include

s a charge storage layer on the gate insulating film, a control gate on the charge storage layer, a cap insulating film on the control gate, and the first side surface of the first stacked gate includes side surfaces of the charge storage layer, the control gate, and the cap insulating film.

3. (Original): The device according to claim 2, wherein the first insulating film is made of a material different from the cap insulating film, and the second insulating film is made of the same material as the cap insulating film.

4. (Original): The device according to claim 2, wherein the contact material has a side surface, the side surface contacts the second insulating film, and a part of the side surface extends over the cap insulating film.

5. (Previously Presented): The device according to claim 1, wherein the first insulating film is an oxide-based insulating film having a film thickness of 100Å to 200Å, and the second insulating film is a nitride-based insulating film having a film thickness of 200Å to 400Å.

6. (Currently Amended): A non-volatile semiconductor memory device comprising:

a semiconductor body of a first conductivity type;

first and second semiconductor regions of a second conductivity type, formed apart from each other on the semiconductor body;

a gate insulating film formed on the semiconductor body between the first and second semiconductor regions and on the second semiconductor region;

a first stacked gate formed on the gate insulating film on the semiconductor body between the first and second semiconductor regions, ~~with a gate insulating film inserted therebetween,~~ the first stacked gate including a charge storage layer on the gate insulating film, a control gate on the charge storage layer, and a cap insulating film on the control gate, and the first stacked gate having a first side surface, a second side surface opposed to the first side surface, and an upper surface, the first and second surfaces each including side surfaces of the charge storage layer, the control gate, and the cap insulating film;

an interlayer insulating film formed above the semiconductor body;

a contact material buried to be adjacent to the first side surface of the first stacked gate in the interlayer insulating film, the contact material contacting the first semiconductor region;

a first insulating film formed on the side surface of the control gate on the first side surface, and on all of the side surface of the charge storage layer on the first side surface, and on the gate insulating film on the second semiconductor region; and

a second insulating film formed on the first side surface adjacent to the contact material, and on the first insulating film on the gate insulating film on the second

semiconductor region, the second insulating film having an etch rate slower than that of said first insulating film ~~and covering the entirety of the first insulating film~~.

7. (Original): The device according to claim 6, wherein the first insulating film is made of a material different from the cap insulating film, and the second insulating film is made of the same material as the cap insulating film.

8. (Original): The device according to claim 6, wherein the contact material has a side surface, the side surface contacts the second insulating film, and a part of the side surface extends over the cap insulating film.

9. (Previously Presented): The device according to claim 6, wherein the first insulating film is an oxide-based insulating film having a film thickness of 100Å to 200Å, and the second insulating film is a nitride-based insulating film having a film thickness of 200Å to 400Å.

10. (Currently Amended): A non-volatile semiconductor memory device comprising:

a semiconductor body of a first conductivity type;

first and second semiconductor regions of a second conductivity type, formed apart from each other on the semiconductor body;

a gate insulating film formed on the semiconductor body between the first and second semiconductor regions and on the second semiconductor region;

a first stacked gate formed on the gate insulating film on the semiconductor body between the first and second semiconductor regions, ~~with a gate insulating film inserted therebetween,~~ the first stacked gate including a charge storage layer on the gate insulating film, a control gate on the charge storage layer, and a cap insulating film on the control gate, and the first stacked gate having a first side surface, a second side surface opposed to the first side surface, and an upper surface, the first and second surfaces each including side surfaces of the charge storage layer, the control gate, and the cap insulating film;

an interlayer insulating film formed above the semiconductor body;

a contact material buried to be adjacent to the first side surface of the first stacked gate in the interlayer insulating film, the contact material contacting the first semiconductor region;

a first insulating film formed on the side surface of the control gate on the first side surface, on all of the side surface of the charge storage layer on the first side surface, on the side surface of the control gate on the second side surface, ~~and~~ on all of the side surface of the charge storage layer on the second side surface, and on the gate insulating film on the second semiconductor region; and

a second insulating film formed on the first side surface adjacent to the contact material, the second insulating film having an etch rate slower than that of said first insulating film and being formed on ~~covering the entirety of~~ the first insulating film, the second insulating film being formed on the second side surface[[,]] and on ~~covering the entirety of~~ the first insulating film on the gate insulating film on the second semiconductor region ~~and the upper surface~~.

11. (Original): The device according to claim 10, wherein the first insulating film is made of a material different from the cap insulating film, and the second insulating film is made of the same material as the cap insulating film.

12. (Original): The device according to claim 10, wherein the contact material has a side surface, the side surface contacts the second insulating film, and a part of the side surface extends over the cap insulating film.

13. (Previously Presented): The device according to claim 10, wherein the first insulating film is an oxide-based insulating film having a film thickness of 100Å to 200Å, and the second insulating film is a nitride-based insulating film having a film thickness of 200Å to 400Å.

14. (Withdrawn) A non-volatile semiconductor memory device comprising:

a plurality of element separation regions made of element separation insulating material buried in a plurality of trenches formed in a semiconductor body;

a stacked gate formed on the semiconductor body between the element separation regions, with a gate insulating film inserted therebetween, the stacked gate including a charge storage layer on the gate insulating film, a control gate on the charge storage layer, and a gap insulating film on the control gate; and

an interlayer insulating film formed above the semiconductor body;

wherein the charge storage layer is provided with a side surface thereof aligned with the element separation regions, and upper surfaces of the element separation regions below

the control gate are higher than the upper surfaces of the element separation regions between control gates.

15. (Withdrawn) The device according to claim 14, further comprising:

a plurality of first semiconductor regions of a first conductivity type, electrically separated from each other by the element separation regions;

second and third semiconductor regions of a second conductivity type, formed apart from each other on the first semiconductor regions;

a contact material buried in the interlayer insulating film, the contact material contacting the second semiconductor region.

16. (Withdrawn) The device according to claim 15, wherein the upper surfaces of the element separation regions between the control gates are lower than an upper surface of the charge storage layer.

17. (Withdrawn) The device according to claim 15, further comprising:

a bit line formed on the interlayer insulating film, for inputting/outputting a signal;

a source line formed on the interlayer insulating film, for inputting/outputting a signal; and

a peripheral circuit including a peripheral transistor, for controlling signals to the bit line, the source line, and the control gate, wherein

the peripheral transistor has a gate insulating film, a gate electrode, a source region, and a drain region, and the gate insulating film adjacent to the contact material connected to one of the source and drain regions has a film thickness smaller than that of the gate insulating film below the gate electrode.

18. (Withdrawn) The device according to claim 17, wherein the stacked gate, the first, second, and third semiconductor regions construct a memory cell transistor, the peripheral transistor is a high-withstanding-voltage-based transistor for driving high voltages for writing and erasure applied to the memory cell transistor during operation of supplying/receiving charges to/from the memory cell transistor, and the gate insulating film below the gate electrode has a film thickness greater than that of the gate insulating film below the charge storage layer of the memory cell transistor.

19 (Currently Amended) A non-volatile semiconductor memory device comprising:

a semiconductor body of a first conductivity type;

first and second semiconductor regions of a second conductivity type, formed apart from each other on the semiconductor body;

a gate insulating film formed on the semiconductor body between the first and second semiconductor regions and on the second semiconductor region;

a stacked gate formed on the gate insulating film on the semiconductor body between the first and second semiconductor regions, ~~with a gate insulating film inserted therebetween,~~ the stacked gate having a first side surface, a second side surface opposed to the first side surface, and an upper surface;

an interlayer insulating film formed above the semiconductor body;

a contact material buried to be adjacent to the first side surface of the stacked gate in the interlayer insulating film, the contact material contacting the first semiconductor region;

a first insulating film made from silicon oxide, formed on the second side surface and on the upper surface and on the gate insulating film on the second semiconductor region, but not on the first side surface of the stacked gate adjacent to the contact material; and

a second insulating film made from silicon nitride, formed on the first side surface adjacent to the contact material and on the first insulating film on the gate insulating film on the second semiconductor region~~, the second insulating film covering the entirety of the first insulating film~~.

20. (New) The non-volatile semiconductor device according to claim 1, further comprising a second stacked gate being formed on the semiconductor body with the gate insulating film interposed between the semiconductor body and the second stacked gate,

wherein the second semiconductor region is located in the semiconductor body between the first stacked gate and the second stacked gate, and wherein each of the first stacked gate and the second stacked gate comprises a charge storage layer on the gate insulating film, a control gate on the charge storage layer, and a cap insulating film on the control gate.

21. (New) The non-volatile semiconductor device according to claim 20, wherein the first stacked gate is comprised in a select transistor, and the second stacked gate is comprised in a memory cell.

22. (New) The non-volatile semiconductor device according to claim 20, wherein the charge storage layer of the first stacked gate and the charge storage layer of the second stacked gate are equal in thickness and use identical material, and wherein the control gate of the first stacked gate and the control gate of the second stacked gate are equal in thickness and use identical material.

23. (New) The non-volatile semiconductor device according to claim 6, further comprising a second stacked gate being formed on the semiconductor body with the gate insulating film interposed between the semiconductor body and the second stacked gate,

wherein the second semiconductor region is located in the semiconductor body between the first stacked gate and the second stacked gate, and wherein the second stacked gate comprises a charge storage layer on the gate insulating film, a control gate on the charge storage layer, and a cap insulating film on the control gate.

24. (New) The non-volatile semiconductor device according to claim 23, wherein the first stacked gate is comprised in a select transistor, and the second stacked gate is comprised in a memory cell.

25. (New) The non-volatile semiconductor device according to claim 23, wherein the charge storage layer of the first stacked gate and the charge storage layer of the second stacked gate are equal in thickness and use identical material, and wherein the control gate of the first stacked gate and the control gate of the second stacked gate are equal in thickness and use identical material.

26. (New) The non-volatile semiconductor device according to claim 10, further comprising a second stacked gate being formed on the semiconductor body with the gate insulating film interposed between the semiconductor body and the second stacked gate,

wherein the second semiconductor region is located in the semiconductor body between the first stacked gate and the second stacked gate, and wherein the second stacked gate comprises a charge storage layer on the gate insulating film, a control gate on the charge storage layer, and a cap insulating film on the control gate.

27. (New) The non-volatile semiconductor device according to claim 26, wherein the first stacked gate is comprised in a select transistor, and the second stacked gate is comprised in a memory cell.

28. (New) The non-volatile semiconductor device according to claim 26, wherein the charge storage layer of the first stacked gate and the charge storage layer of the second stacked gate are equal in thickness and use identical material, and wherein the control gate of the first stacked gate and the control gate of the second stacked gate are equal in thickness and use identical material.